National Aeronautics and Space Administration

Evaluation Methodology Guidance for Stack Packages

Reza Ghaffarian, Ph.D.
David Gerke, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 09-23 10/09

National Aeronautics and Space Administration

Evaluation Methodology Guidance for Stack Packages

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Reza Ghaffarian, Ph.D.
David Gerke, Ph.D.
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 939904.01.11
JPL Project Number: 103982
Task Number: 03.03.12

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

http://nepp.nasa.gov

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Objectives and Products

This report provides evaluation methodology guidance based on previous National Aeronautics and Space Administration (NASA) reports and literature surveys for 3D stack packages and assemblies. Two aspects of technology are covered: the package itself (guidance for functional packages) and package assembly manufacturing and reliability. This work was funded by the NASA Electronic Parts and Packaging (NEPP) Program. The objectives of this NEPP project are to:

- Perform a literature survey of 3D stack technology.
- Perform a literature survey on the evaluation methodology for 3D package and assembly.
- Combine the two aspects to provide evaluation methodology for both aspects with consideration of interactions between package and assembly.
- Generate guidance on the evaluation methodology for 3D stack package integrity prior to and after assembly.
- Provide recommendations on future experimental activities.

The qualification and evaluation methodology guidelines will facilitate NASA projects in effectively evaluating the reliability of very dense and newly available high-density 3D stack packages, allowing more processing power in a smaller board footprint and lower system weight.

Table of Contents

1. Organization and Topics of Report

This report provides a body of knowledge (BoK) survey for 3D stack packages covering package technologies and evaluation methodologies. Topics discussed in this report are as follows:

- Executive summary providing key 3D stack technology trends and newly available commercial-off-the-shelf (COTS) 3D packages.
- Summary of key test results on a specific 3D package previously evaluated by National Aeronautics and Space Administration (NASA) / European Space Agency (ESA) for space applications.
- Review of key evaluation methodologies for single die packages as a baseline (since data for 3D packages are missing) and additional specific qualifications required for 3D packaging technology and assembly.
- Discussion of packaging challenges, including heat dissipation at package level and warpage at assembly level—two key limitations for 3D integrated circuit (IC) packaging technology.
- Summary of key findings for NASA applications and recommendations for future studies to determine key quality and reliability indicators for 3D stack technology.

2. Executive Summary

Stack packaging—more than Moore—has recently become very attractive for use in commercial electronics because of cost and limitation of die fabrication with finer features. Moore's law, stating that the number of transistors on a given chip will double every two years (now 18 months), has been substantiated and implemented throughout the past three decades. The exponential growth for die density has allowed computers and electronic communication devices to become cheaper and more powerful simultaneously. In addition, the increase in package density has further helped this miniaturization trend by using area array for interconnection rather than conventional packaging such as quad flat pad (QFP) with peripheral leads. A package with an array of solder bumps is commonly referred to as ball-grid array (BGA) technology. If the package dimensions are nearly those of the integrated circuit (IC) itself, then the technology is called chip-scale packaging (CSP). Wafer-level package (WLP) uses wafers with added protection coating, and subsequent singulation provides dense components with standard packaging attributes such as ease of testing and handling.

Figure 1 illustrates stack packaging trends from those that are in the development stage to those that are now mainstream. Currently, 3D packaging consists of stacking of packaged devices called package-on-package (PoP), including through-mold via (TMV™), and stacking of die within a package called package-in-package (PiP) or stacked wire-bonded die (primarily memory). The PoP and PiP technologies are used today using conventional stacking or other unique technologies such as TMV™ and through-silicon via (TSV) as well as through-edge-interconnection processes for device stacking within packages.

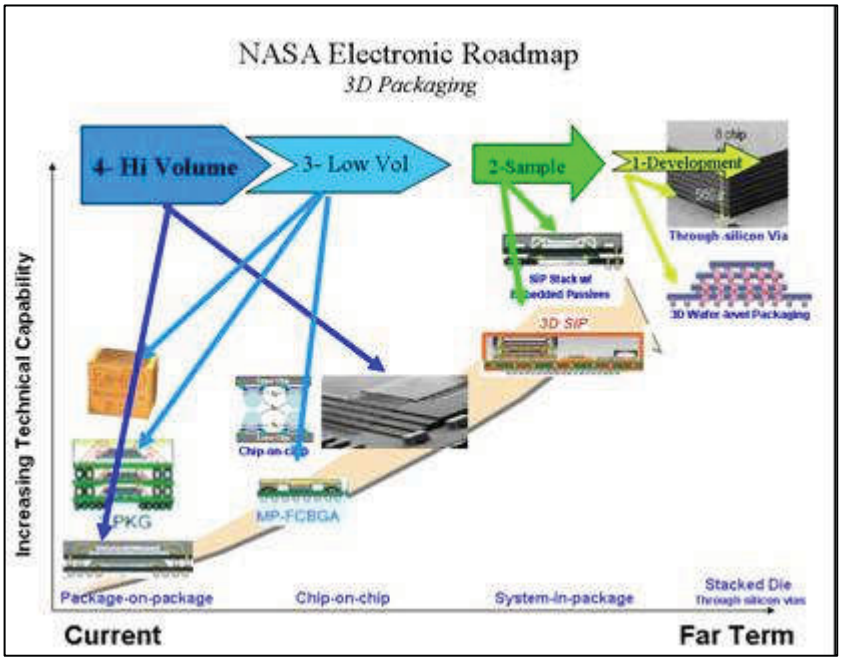

Figure 1. 3D stack packaging technology roadmap with maturity status.

An expert from one of the largest commercial-off-the-shelf (COTS) package suppliers [1] states that in the past "packaging has been a contributor but not a key enabler"; however, there is a paradigm shift in which "the 3rd dimension will be the key enabler and supply chain maturity will determine the speed of adoption." He defines several key limiting factors in supply chains, including equipment to handle very thin die, thermal management solution, test technology to ensure quality and reliability, and technology for die-to-die and die-to-wafer bonding. He identifies miniaturization as the near-term driver for 3D/TSV, with performance improvement as the mid-term driver, and cost reduction through elimination of wire bond assembly as the long-term driver.

In general, COTS conventional or 3D packages using plastic-encapsulated materials (PEMs) have two key limitations:

1. Due to the major differences in design and construction, COTS packages have a smaller operating temperature range and are typically more frail and susceptible to moisture absorption compared to high-performance devices; therefore, the standard test practices used to ensure that high-performance devices are robust and highly reliable often cannot be applied to PEM packages.
2. Users of 3D COTS packages have little visibility into commercial manufacturers' proprietary design, materials, die traceability, and production processes and procedures, whereas controls are in place for the high-reliability systems.

Currently, only an extremely limited number of manufacturers supply 3D stack packages for use in high-reliability applications. These stack packages come in the form of ceramic packages with peripheral lead configuration for solder joint assembly (even though stacking may have been performed by area array or edge interconnections). Leaded packages provide acceptable long-term solder joint reliability required for such application. Assembly of COTS 3D-stack area array packages is more challenging and a number of industry investigators have performed tests to address their issues for commercial applications. However, reliability evaluation is yet to be performed to address more stringent requirements for high-reliability applications.

A literature survey, discussed in detail in the body of this report, indicated that most prominent failures for COTS 3D packages and assemblies are due to warpages (individual or system) for plastic packages. For the stack ceramic package and TMV™, failures due to via are of concern. In addition, both plastic and ceramic stack packages are required to meet minimum shock and vibration requirements per Mil-STD-883. Separation of stack layers, if not adhesively bonded together, during shock is another failure mechanism that needs to be considered. In addition, very limited techniques are available to ensure quality and reliability of 3D stack packaging and assemblies.

This report provides an overview of 3D stack packaging trends from wire-bonded stack within packages to stack area array packages. Evaluation methodologies and package assembly challenges and key reliability issues are also reported. Packaging qualification methodologies and evaluation for space parts—military and commercial—are well established; therefore, any new evaluation methodology and deviation (upscreening) from established limitations other than those recommended by package suppliers may void the vendor's certification. The added evaluation may be required to mitigate risks for the PEM and 3D stack technologies. However, for assembly, it is the norm to establish additional process controls to achieve acceptable assembly quality and workmanship.

This report includes applicable methodologies and evaluation test approaches specifically defined for 3D stack packages and assemblies. Specific procedures for testing of PEM and COTS 3D packages to meet NASA requirements are discussed in detail. This report also provides recommendations for future activities on 3D stack technology to address specific needs for high-reliability applications.

3. Literature Survey

3.1 Introduction

The demand for high-frequency operation, high-input/output (I/O) density, and low parasitics as well as the need for package-level integration with small form factors and extreme miniaturization have led to numerous new packaging technologies. The new packages combine flip-chip and wire-bond interconnection, build-up, and laminate substrates, and bring about package-level integration of disparate device functions through 3D die and package stacking.

Of the existing commercial-off-the-shelf (COTS) 3D packaging technology options, wire-bonding remains the most popular method for low-density connections of less than 200 I/O per chip. In the near future, however, it will become difficult to meet the increasing frequency requirements and demands for wiring connectivity merely by increasing the number of the peripheral wire-bonds. In order to overcome such wiring connectivity issues, 3D chip stacking technology using through-silicon vias (TSVs) is attractive because it offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance.

A recent presentation by two key industry experts in COTS package technologies [1, 2] revealed industry roadmaps and requirements for 3D integrated circuits (ICs) and systems for 3D packaging. Both experts agree that mobile phones are the largest single-volume driver for advanced COTS electronics packages—more than one billion shipments in 2009 despite downturn. Increase in functionality with small form factors are achieved using stack-die chip-scale packages (CSPs), package-on-package (PoP), system/package-in-package (PiP), embedded components, and TSV for camera modules. The following summary provides a status of COTS 3D stack packages:

- 3D packages are in high-volume production
  - Stacked die packages (PiP)
  - Stack packages (PoP)
- 3D TSV technology has been demonstrated
  - More than 50 organizations identified with 3D TSV
- Cost/performance trade-off determines 3D package type adoption
  - Image sensors are in production today
  - High-speed logic (processors, field programmable gate arrays [FPGAs])
  - Memory (flash, dynamic random access memory [DRAM], synchronous dynamic random access memory [SDRAM]) future, depends on cost trade-off
- Issues remaining for 3D ICs
  - Design software needs to be ubiquitous to chip designers
  - Thermal issues
  - Test issues require cost-effective solutions

Several industry experts also discussed 3D TSV under “The Packaging Summit,” in the recent August 2009 Semicon West Conference and Exhibition [27]. In support of 3D ICs, Tom Gregorich, Vice President of IC Package Engineering, Qualcomm, in his presentation entitled “3D Semiconductor Integration: Holy Grail or Industrial Myth?” defined the following key issues regarding electronics density shrink and performance challenges:

- Scaling is nearing the end of the road; with dies continuing to shrink, it is becoming more difficult to get increasing value out of the wafers.
- Bus speeds and bus widths are continuing to increase and without new technology, the performance requirements cannot be handled.
- Scaling is a means not an end—the goal of scaling is cost reduction and/or performance improvement and 3D ICs will only replace scaling if it is better or cheaper.

3.2 Packaging Trends

3D packaging is a response to the demand for high-frequency operation, high-I/O density, and low parasitics as well as package-level integration with small form factors and extreme miniaturization. 3D packaging allows package-level integration of disparate device functions that combine flip-chip and wire-bond interconnection, build-up, and laminate substrates. Of the existing 3D packaging technology options, wire bonding remains the most popular method for low-density connections of less than 200 I/O per chip. In the near future, however, it will become difficult to meet the increasing frequency requirements and demands for wiring connectivity merely by increasing the number of peripheral wire-bonds. In order to overcome such wiring connectivity issues, 3D chip and stack packaging technology using TSV and through-mold via (TMV™) are attractive as they offer the possibility of solving the serious interconnection problems at die and package levels while offering integrated functions for higher performance.

For high-density packaging, the migration to 3D has become mainstream. Figure 2 illustrates the various 3D stack technologies. The technologies are categorized by package style, based on assembly robustness, area array and leaded packaging, and die within ball grid arrays (BGAs) / CSPs including wire bond, flip chip, and TSV. 3D packaging also consists of stacking of packaged devices, known as PoP, and stacking of die within a package, known as PiP or system-in-package (SiP). Both PoP and PiP technologies are used today with the promise of TSV technology for die stacking. For the PoP technology, another approach, TMV™, is now being implemented to provide interconnections for the 3D packages. The following sections provide further discussions on specific 3D packaging technology.

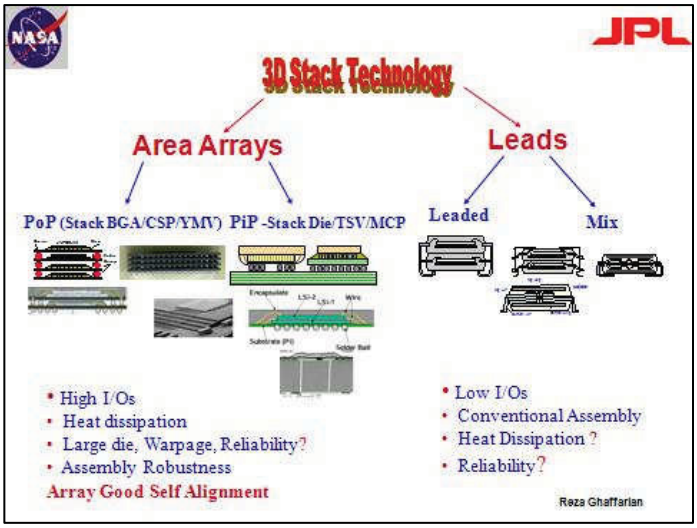

Figure 2. 3D stack packaging technology types, area array, and leaded packages with various stack configurations both internally and externally.

3.3 Package-on-Package (PoP)

PoP is a packaging technology placing one package on top of another to integrate different functionalities while still remaining compact in size. This packaging technology offers procurement flexibility, lower cost of ownership, better total system costs, and faster time to market. Normally, designers use the top package for memory application and the bottom package for application-specific integrated circuits (ASICs), baseband, or processor applications. By using this technology, the memory known-good-die (KGD) issue can be mitigated since the memory to be integrated with the bottom package can be burned-in and tested before integration. PoP also answers issues with wafer thinning, die attach, wire bond, and thermal dissipation.

3.3.1 PoP: Center Mold and Flip Chip

Back as far as 2002, a PoP was developed for a camcorder application by Advanced Semiconductor Engineering, Inc. (ASE). Initially, the chip was packaged in a special PoP with an interposer between the two packages to accommodate the thick (0.53mm) glob top on the bottom package (shown in Figure 3a). The product was then redesigned to remove the interposer for further total package height and cost reduction by using the transfer molding process as shown in Figure 3b.

Other center packages/die types include Amkor package stackable, very thin fine-pitch BGA and flip-chip CSP (PSvfBGA/PSfcCSP) [3]. For PSfcCSP, the package is replaced with an exposed flip-chip die. For PSvfBGA, an extremely thin mold cap is required to support the fine-pitch, top-memory package with an estimated 0.25 mm raw-ball diameter. This requires an extremely thin (<50 µm) die whether as flip-chip or wire-bonded, which would raise package assembly process and cost challenges. Furthermore, <50 µm is well below the die thickness at which IC suppliers characterize complementary metal oxide semiconductor (CMOS) and systems-on-chip (SOC) technologies for electrical integrity across thermal and mechanical stresses. Die thickness characterization is critical for PiP system devices that integrate sensitive analog or memory circuits. It is critical that the thin die be characterized with each new CMOS process node and within the package type(s) or application(s) that exhibit the highest stresses on the die.

Similar issues also exist for the flip-chip version, PSfcCSP package. This stack configuration also requires an extremely thin die and low-bump standoff, raising similar package assembly and die characterization issues as noted above. In addition, thin exposed die have handling challenges through final test and surface mount technology (SMT) processing that can affect yield and quality due to die-crack or die-edge chip outs common with exposed flip-chip die package structures.

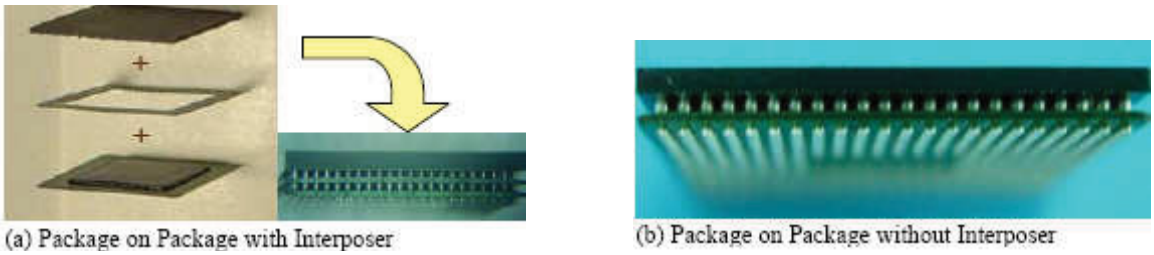

Figure 3. (a) Package-on-package (PoP) with initial use of interposer and **(b)** new version with no interposer (Advanced Semiconductor Engineering Inc. and MEMS Institute, Taiwan).

PSvfBGA center mold structure limits the maximum die that will mechanically fit in a given package size due to the distances required from mold cap edge to stacking pad edge and die edge to mold edge. PSfcCSP, due to underfill fillet and resin bleed control, also limits the maximum die size between stacking lands. Other issues include warpage challenges for both PSvfBGA and PSfcCSP because of the unbalanced coefficient-of-thermal-expansion (CTE) mismatched nature of their structures that can limit the ability to incorporate thin substrates. Warpage control requirements, both coplanarity and high-temperature (Pb free) soldering profiles, will be tight to meet the current SMT infrastructure.

The PSfcCSP structure does not support stacked die configurations where one or more tiers of wire bonds are required. PSvfBGA supports stacked die configurations in production but may require a much thicker mold cap, which is not viable for PoP stacking pitches below 0.65 mm without significant reduction in die thickness or adoption of new SMT stacking technology.

3.3.2 PoP with Partial Cavity Structure

Due to these challenges, the industry has been evaluating new bottom package structures to address the high-interconnect density challenges associated with the newer emerging PoP applications. One includes use of partial cavity organic laminate substrates so that the die is attached to a routing layer below the top layer where the PoP stacking lands are fabricated. This allows a thicker die and more clearance from the thin mold cap to die top surface. However, the substrate fabrication infrastructure for this type of partial cavity design is immature, limiting the availability of supply, and making the design, development, and unit costs very high for early adopters of this technology. Amkor [3] has been evaluating partial cavity substrate supply for more than seven years without seeing commercial viability of this technology for PoP in cost-sensitive applications, such as smart phones and consumer electronics. Furthermore, warpage profiles for this technology raise concerns for package assembly with thin die, as well as SMT stacking for fine-pitch interface requirements.

3.3.3 PoP: Through-Mold Via (TMV™)

TMV™ uses a matrix-molded platform for bottom PoP construction and creates through-via interconnections to the top surface via a laser ablation process [3]. Figure 4 illustrates the key elements of the bottom TMV™ PoP developed by the package supplier for their internal qualification and joint SMT studies. The 14×14 mm daisy chain package incorporates a 200 I/O, 0.5 mm pitch top side interface, and 620 bottom BGAs at 0.4 mm pitch.

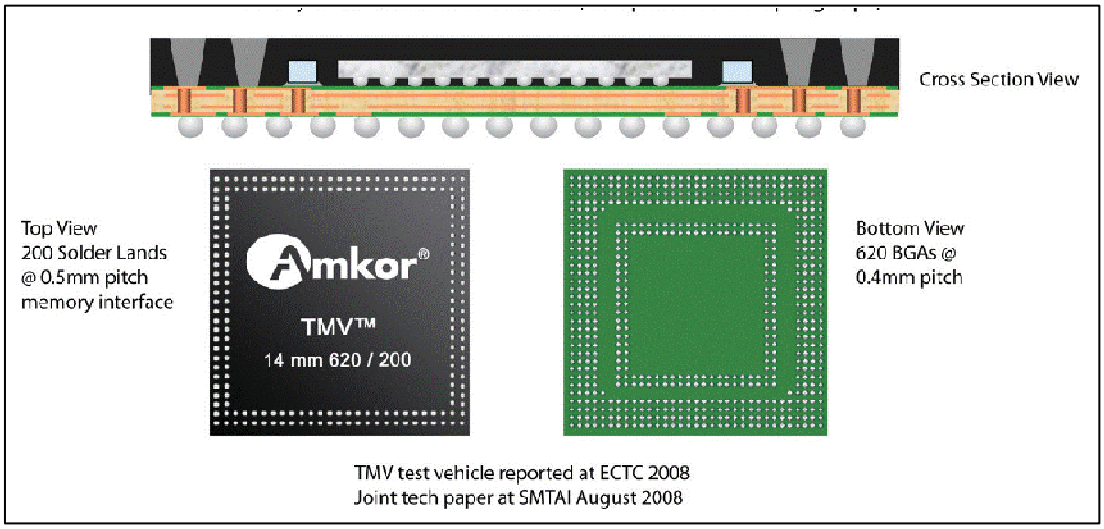

Figure 4. Cross-section top and bottom view of a new TMV™ PoP package [3].

The benefits of TMV™ technology include the following:

- Removes the pitch vs. package clearance bottlenecks to support future memory interface density requirements enabling the memory interface to scale with CSP pitch reduction.
- Improves warpage control and bottom package thickness reduction requirements by utilizing a balanced fully molded structure.
- Provides an increased die-to-package size ratio.
- Supports wire bond, flip chip, stacked die, and passive integration requirements.
- Leverages strong technology roadmaps and high-volume scale, from fine-pitch ball grid array (FBGA), stacked die, flip-chip CSP, and SiP platforms.
- Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- Expected to improve board-level reliability of the stacked memory interface using rules developed by package supplier.

Improvement in warpage behavior with thermal profile was shown in comparison to PSfcCSP, both from the same package supplier [3]. Thermal shadow moiré testing was performed to evaluate the warpage behavior for the two packages. The TMV™ PoP package exhibited a dramatic improvement in warpage compared to the conventional PSfcCSP package, as shown in Figure 5. Samples for TMV™ were built with the extremely thin core, four-layer 0.21mm thick substrates, whereas a thicker 0.3mm substrate was required to reduce warpage for stack PSfcCSP test vehicles. However, even with the thicker substrate, the warpage exceeded the commercial requirements for PoP stacking with the PSfcCSP samples.

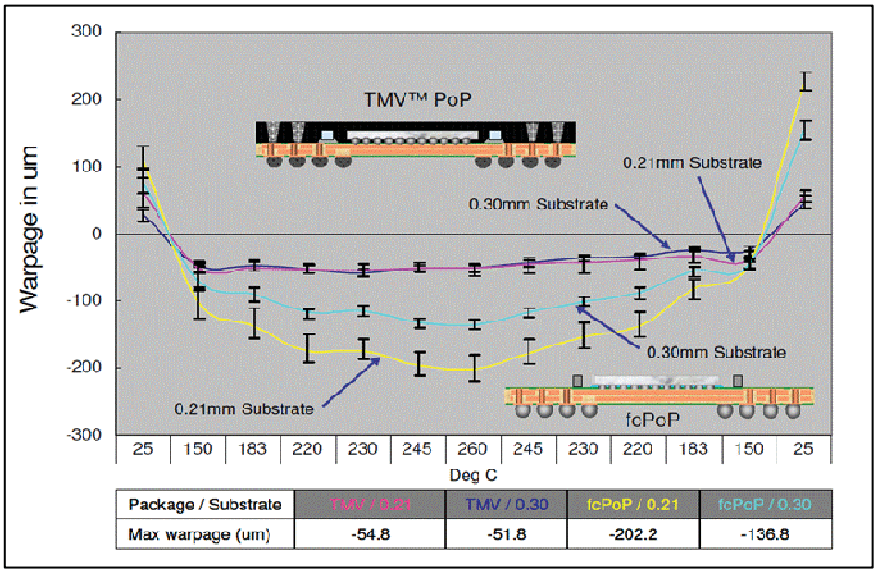

Figure 5. Thermal shadow moiré results for TMV™ and PSfcCSP PoP packages [3].

3.4 Package-in-Package (PiP)

Handsets and other mobile handheld products are defining a new application for packaging technology that goes beyond the realm of traditional packaging. The optimum solution often lies in a judicious combination or hybridization of these seemingly dissimilar technologies and approaches. One such package is often called PiP. One particular example of this technology is comprised of the integration of three key functions, which form the engine of a high-end cellular communication device into a single package, i.e., a baseband digital signal processor (DSP), a high-speed local memory, and an analog device that couples with the DSP.

The DSP and analog devices are featured as individual die obtained from sorted good wafers, whereas the memory device is procured as a pre-tested package in a proprietary land grid array (LGA) format known as the internal stacked module (ISM) [3]. The pre-tested ISM configuration for memory (as opposed to a bare die) ensures that the devices are electrically good before being put into the package, thereby reducing the potential fallout of the finished package due to marginally functional memory die. The DSP is packaged as a flip chip in order to meet the high-I/O density and performance requirements. Since the memory is provided in a pre-packaged, pre-tested form (ISM), the package structure is described as flip-chip PiP with a Joint Electron Device Engineering Council (JEDEC) designation of fcLFBGA-PiP-SD2+1. Figure 6 shows the example discussed here.

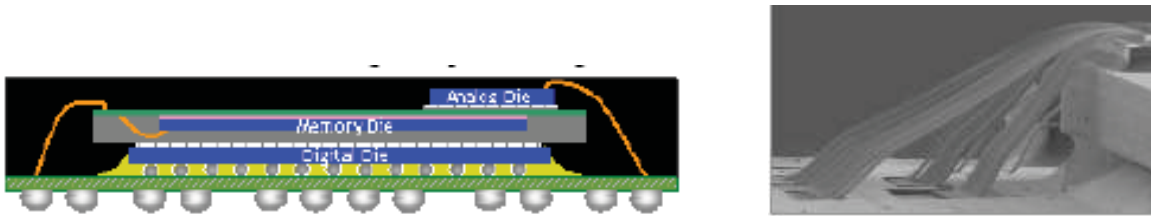

Figure 6. Side view sketch of PiP and SEM showing wire bonds used in the PiP example (STATSChipPAC Inc. and Qualcomm Inc.).

3.4.1 PiP: Wire-Bonded Stacked Die

Vertical chip stacking can be performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Stacked die products inside a package results in the thinnest package with the highest board-level reliability and lowest assembly cost. Most of the time, stacked die are multiple memory chips and rarely mixed device types, such as stacked memory with logic devices added. Special low-profile wire bonding has been developed and is a critical process for this technology.

Stacked die concepts utilizing silicon spacers or epoxy filled with spherical spacers have been used. In the silicon-spacer concept, a thin piece of silicon is used to separate the active dies in the stack. In the glue-spacer concept, this is accomplished with a spherical-filled die-attach. Adding silicon into the package increases the bending resistance. Associated with this is the increased risk and/or propensity for cracks during assembly and/or reliability / qualification testing, either in the package body (molding compound) or in the die itself.

3.4.2 PiP: Wire Bond and Flip Chip

Flip-chip bonding is also used in PiP interconnection, either on its own or as a complement to wire bonding as shown in Figure 7. Flip-chip configuration may be applied to either the upper die or the lower ones, depending on the intent of the design. Flip chipping a bottom die directly onto the substrate enables that die to operate at a high speed. On the other hand, flip chipping a top die eliminates the use of long wires for connection to the substrate.

3.4.3 PiP: 3D Wafer-Level Package with FC/TSV

Figure 8 shows concepts for 3D wafer-level, chip-scale package (WLCSP) technology [4] that combines face-to-face bonding of fine-pitch, flip-chip components and low-profile passives onto a redistribution layer of another silicon component (a WLCSP). In this manner for example, a flip-chip driver can be mounted directly onto a CSP memory component, ASIC, etc. Yield and reliability of a number of these packages were investigated and it was found that the finer pitch, active component showed slightly lower yields than the courser pitch. Reliability results indicated that the underfill selection had a large impact on the reliability of the 3D WLCSP. The higher reliability capillary underfills tended to have higher modulus and lower CTEs relative to the lower reliability materials.

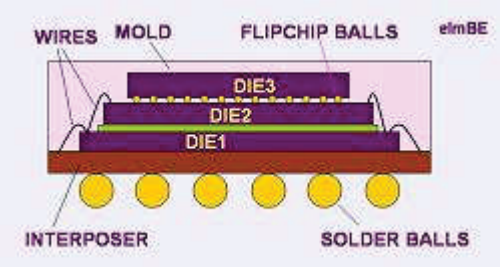

Figure 7. Example of a 3-die PiP configuration employing both wire bonding and flip-chip bonding.

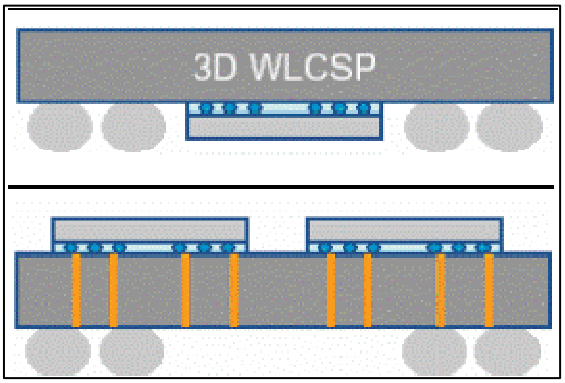

Figure 8. 3D WLCSP concepts.

3.4.4 PiP: Through-Silicon Via (TSV)

This category of packages with TSV stack die is often called "3D integration" in order to distinguish them from 3D packaging. Stacked memory die is the perfect choice for using TSV technology as all interconnections of each die align with the corresponding die located above and below. However, this is merely a building block for future designs as mobile terminals to supercomputers, which require maximum computing power using limited resources such as power consumption and volume for next-generation information processing devices. A 3D-integrated logic device with stacked memory matches this objective because the shortest and highly parallel connection between logic and high-capacity memory reduces the power consumption due to long-distance and high-frequency signal transmission, and realizes the highest device density.

3.5 Non-Conventional 3D Technology

Recently, in addition to embedding passive components, attempts are being made to embed active chips. For the embedded active structure, thinned active chips are directly buried into a core or high-density interconnect layers, as opposed to placed on the surface. Currently, active chips can be embedded in many different ways within the categories of chip-first, chip-middle, and chip-last depending on the approaches involved. Embedding is expected to reduce the parasitic effects of interconnects (reduced interconnect length) resulting in lower power dissipation, and to provide better electromagnetic shielding. They also offer smaller and thinner package profiles.

The performance benefit of embedded chip build-up (ECBU) packaging technology [5] was compared to commercial high-performance flip-chip solder attach on high-density organic chip carriers. In general, the chip-first technology has a number of challenges:

- The chip, once it is embedded, is subjected to a number of processing steps and can be affected due to the fabrication.
- Serial chip-to-build-up processes accumulate yield losses associated with each process.
- Defective chips cannot be easily reworked in current embedded package structure. Thus, this technology needs 100% known good die (KGDs).

- The interconnections in the chip-first approach, which are direct metallurgical contacts, can encounter fatigue failures due to thermal stress.
- Thermal management issues are also evident since the chip is totally embedded within polymer materials during substrate or build-up layer processes.

National Aeronautics and Space Administration (NASA) Jet Propulsion Laboratory (JPL) and Auburn University collaborators [6] evaluated ultra-thin flexible microelectronics by embedding less than 50 μm silicon die for use in applications such as conformal and wearable electronics. As shown in Figure 9, three techniques have been developed to fabricate ultra-thin, flexible electronics: 1) thinned die flip-chip bonded on polyimide or liquid crystal polymer (LCP) flex, 2) thinned die laminated into LCP films, and 3) thinned silicon die embedded in polyimide. The manufacturing methods and materials for each of these approaches is described in the following sections.

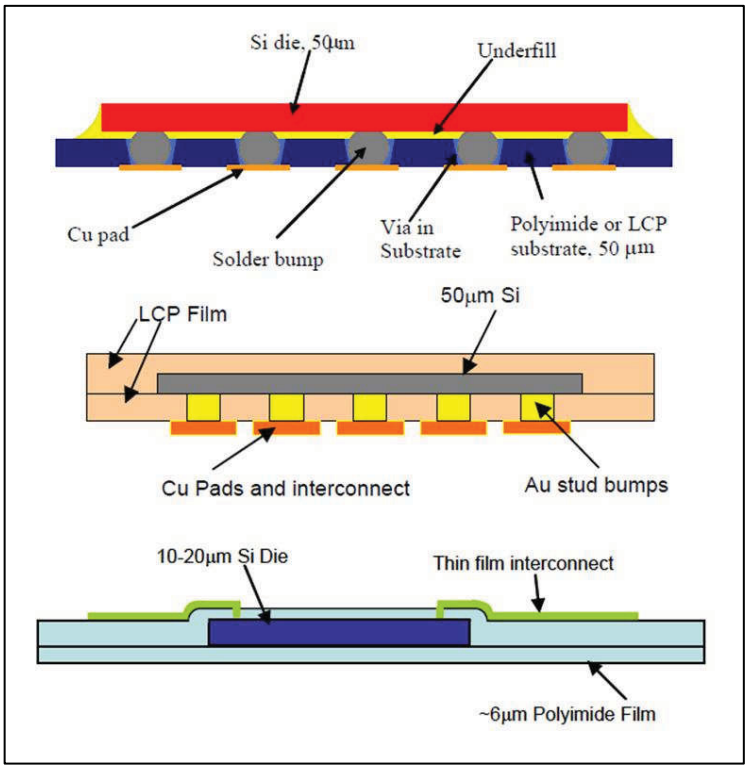

Figure 9. Three techniques of thinning die: polyimide and LCP substrate with solder assembly (*top*); LCP substrate with thermal compression bond Au stud bump assembly (*middle*); thinned Si die embedded in polyimide with thin film interconnect (*bottom*).

4. High-Reliability Applications

4.1 3D Plus Stacked Plastic Packaging

4.1.1 Joint Testing Performed by NASA, ESA, and CNES

3D Plus processes, using specially designed test structures, were evaluated cooperatively by the European Space Agency (ESA), Centre National d'Etudes Spatiales (CNES), 3D Plus, and National Aeronautics and Space Administration (NASA) Goddard Space Flight Center (GSFC) [7, 8]. The testing and design of the evaluation structures were intended to explore the ability of the process to produce rugged, stacked, electronic devices that survive typical conditions of space flight use. The layers of the stack include additional special devices for detecting numerous device and package characteristics, including (1) moisture ingress, (2) torsion stress during temperature changes, (3) stacking effect on chip resistors and capacitors mounted on the same layer as silicon devices, (4) stack design effect on typical memory chips, both packaged and in die form, and (5) heat dissipation behavior of the cube without an internal heat sink.

4.1.2 Test Plans

ESA and CNES managed the portion of the test plan that included the following tests:

- Preconditioning thermal (cycling) vacuum
- 500× thermal cycling (-55°C to +125°C)
- Temperature humidity bias (+85°C/85%RH/1000 hrs)
- High temperature bake (+125°C, 2000 hrs)
- Power cycling (30 k × on/off, 120 sec on +110°C, 60 sec off +40°C)

NASA/GSFC provided the following tests:

- CSAM, µfocus X-ray
- Thermal conditioning (+125°C, 48 hrs)
- Voltage conditioning (+125°C, 320 hrs)
- Thermal characterization
- Vibration (sine & random)
- Mechanical shock
- 85% humidity / 85°C
- Finite element modeling

4.1.3 Results of NASA/ESA Tests on 3D Stack Packages

The following results were reported [7, 8]:

- Corrosion monitor resistance: The data was consistent over the testing, though some of the tracks on layer 10 baselined higher than those on layer 1. Layer 10 was also slightly more sensitive to moisture.

- Corrosion monitor isolation: The data was all within specification though layer 10 seemed to be more sensitive to moisture (85/85 test). The sensitivity to the vibration tests may have also been moisture related as those tests were conducted during the most humid time of the year.
- Contact continuity: All measurements showed continuous circuits with no significant sensitivity to moisture.
- Daisy-chain wire bonds: All measurements showed continuous circuits with no permanent sensitivity to moisture or other environment-induced changes.
- Strain gauge: The dice in FM3 showed a sensitivity to temperature while the dice in FM9 and FM10 did not. No failure trends were encountered over the mechanical and moisture testing. FM5 had a failure during baseline electrical and voltage conditioning (see above).
- Thermal monitor, Vf, 0V, and 12V on heaters: No out-of-family data was encountered. No difference could be detected between the layer with and without a heat sink.
- Thermal monitor, IR, 0V, and 12V on heaters: One device was received in a failed condition (see above). For the remaining data, no out-of-family data was encountered. No difference could be detected between the layer with and without a heat sink.
- Capacitors: No significant change occurred over all tests.
- Resistors: All measurements were within specification.
- Dynamic random access memory (DRAM): A failure was apparent following thermal characterization and sine vibration, which continued through the subsequent random vibration test (noted above). All other measurements were within specification.

It was reported that the 3D Plus packaging technology provides very high-density and stable performance in rugged environments. The parts were found to be suitably rugged with respect to high and low temperature, humidity, shock, and vibration. The data did not indicate that there was a need for special moisture protection even though these packages are non-hermetic. Care should still be given to keep the parts as dry as possible to ensure long life. No significant performance difference was noted between the layer with the heat sink and the one without the heat sink. The results for the temperature cycling and long-term temperature tests were similarly stable for all of the layers [8].

The test vehicles were exposed to severe environmental stress and thousands of passing data points were collected indicating that this technology is highly suited for use in extreme environments where normal derating and protection practices, for temperature and moisture, are used. It was also noted that care must be taken to properly stake the parts as the aspect ratio of height to width is high.

4.2 3D Stack EEPROM Rad Hard

Radiation-hardened microelectronic components, including 3D stack electrically erasable programmable read only memory (EEPROM) and single board computers are available to the space community [9]. High-performance commercial semiconductors are screened and then

protected through proprietary radiation mitigation technologies to provide turnkey radiation-hardened product solutions as patented RAD-PAK® and XRAY-PAK® packages. Figure 10 summarizes the EEPROM packaging technology. The packages are qualified to MIL-PRF-38535, Class Q, and Class V. Many are manufactured using MIL-PRF-38534 as a guideline and screened to manufacturer self-defined Class H and Class K flows.

Figure 10. 3D EEPROM rad shield technology for space applications.

5. Evaluation Methodologies for Stack Packages

The advantages of commercial-off-the-shelf (COTS) 3D stacking technology are numerous and for that reason this technology is widely adopted by industry for various applications with higher density requirements. Disadvantages can be divided into two key areas: the necessity for a robust evaluation development for screening of these complex packaged devices and development of additional optimization required to achieve a successful package assembly.

Plastic encapsulated microcircuits (PEMs) are considered for use over traditional ceramic parts in telecommunications, avionics, military, and space applications when their significant advantages in size, weight, cost, availability, performance, and state-of-the-art technology are prevalent. For space applications, use of plastic parts is a means to make available advanced technology functions. Confidence developed for hermetic devices does not automatically apply to plastic-packaged devices. Key challenges in implementation for high-reliability applications have been the subject of many investigations [10–13].

Potential users of PEMs need to be reminded that unlike the high-reliability devices and microcircuits that are designed to perform reliably in a variety of harsh environments, PEMs are primarily designed for use in benign environments where equipment is easily accessed for repair or replacement. The methods of analysis applied to military products to demonstrate high reliability cannot always be applied to PEMs. This makes it difficult for users to characterize PEMs for two reasons:

1. Due to the major differences in design and construction, the standard test practices used to ensure that military devices are robust and have high reliability often cannot be applied to PEMs that have a smaller operating temperature range and are typically more frail and susceptible to moisture absorption. In contrast, high-reliability military microcircuits usually utilize large, robust, high-temperature packages that are hermetically sealed.
2. Unlike a military high-reliability system, users of PEMs have little visibility into commercial manufacturers' proprietary design, materials, die traceability, and production processes and procedures. There is no central authority that monitors PEM commercial product for quality, and there are no controls in place that can be imposed across all commercial manufacturers to provide confidence to high-reliability users that a common acceptable level of quality exists for all PEMs manufacturers. Consequently, there is no guaranteed control over how much reliability is built into commercial product, and there is no guarantee that different lots from the same manufacturer are equally acceptable. Regarding application, there is no guarantee that commercial products intended for use in benign environments will provide acceptable performance and reliability in harsh space environments.

The key advantages of plastic-packaged parts over hermetic-packaged parts include the following:

- Typically, there is no internal cavity and all internal parts are supported by rigid plastic encapsulants. Therefore, there is improved performance under severe mechanical shock and vibration (for example, during launch).

- There are no internal particles from solder, wires, sealing glass, etc., which might cause intermittent shorting.
- Internal lead wire sag, permitting the shorting of wires to the edge of the silicon chip, is eliminated.

These issues as well as evaluation methodologies are discussed in the following sections.

5.1 COTS PEM Single/3D

5.1.1 PEM Molding Materials Use Limitation

PEMs are epoxy-based resin mixtures and are low-temperature materials compared to glasses and ceramics used in military-style hermetic packages. This may restrict PEM usage in some high-temperature applications. Plastic molding compound (following industry custom, this is designated epoxy mold compound or EMC) is a complex proprietary formulation of a specific encapsulating resin (usually novolac cresol epoxy resin) and various types of additives that provide the desired properties for the packaged device. Formulations include hardening compounds, accelerators, fillers, flame retardants, couplers, mold-release additives, coloring, and ion-getters. Fillers (crushed electronic grade Silica–silicon oxide is most often used) have a significant effect on reliability through lowering the temperature coefficient of expansion of the encapsulant so as to be closer to that of the silicon die, lead frame, and bond wires. A significant property of the EMC is ionic purity, which has been shown to be important for device reliability.

5.1.2 Outgassing of Plastic Packages

Outgassing is a concern in space missions, particularly in an enclosed container, where volatile materials may condense on sensitive optical surfaces. Outgassing testing has been used to identify and quantify volatiles being emitted from PEM samples according to American Society for Testing and Materials (ASTM) E595 (Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment). The parameters measured for this standard are the total mass loss (TML), collected volatile condensable materials (CVCMs), and the water vapor regained (WVR). Since molding formulations may change with part manufacturer and technology, outgassing tests may need to be done to ensure PEM suitability for critical space applications.

5.1.3 Moisture Absorption

Epoxy resin and EMC are inherently hygroscopic—they absorb moisture. PEMs have a failure mechanism not present in hermetic parts—damage due to printed circuit board (PCB) assembly, soldering, and cleaning. Moisture-induced package damage (such as interfacial delamination and cracking during solder reflow) can be a major reliability problem. Collectively, these phenomena are known as popcorning. Surface mount devices (SMDs) are more susceptible to this problem than through-hole parts because they are exposed to higher temperatures during reflow soldering. The soldering operation must occur on the same side of the board as the SMD. For through-hole devices, the soldering operation occurs under the board thus shielding the devices from the hot solder. SMDs have a smaller minimum plastic thickness from the chip-to-mount-pad interface to the outside package surface; this difference

in thickness has been identified as a critical factor in determining moisture cracking sensitivity. Because of this problem, PEM storage requirements to be followed for SMDs have been generated by manufacturers. Storage is determined by experimental measurements of moisture uptake at various conditions of relative humidity and temperature and geometrical EMC strength.

5.1.4 Glass Transition Temperature

Glass transition temperature (Tg) is the point at which a substance changes from a hard glassy material to a softer rubbery one. For cross-linked thermosetting polymers (such as EMC used in PEMs), the transition occurs across a band of temperatures. Figure 11 illustrates a number of Tg graphs generated by the thermal mechanical analysis (TMA) method. The mismatch between coefficient of thermal expansion of the EMC and other PEM internal materials above the glass transition temperature will cause significant stress buildup in packaged components during mission applications, possibly leading to early device failures. Because of this, the Tg of the PEM should not be exceeded during mission use.

5.1.5 Pure Tin Plating and Tin Whiskers

Many PEMs have pure tin-plating, lead coating only. This condition has significant risk of electrical anomalies (shorts) due to growth of tin whiskers. Each flight lot should be evaluated for the pure tin-lead coating.

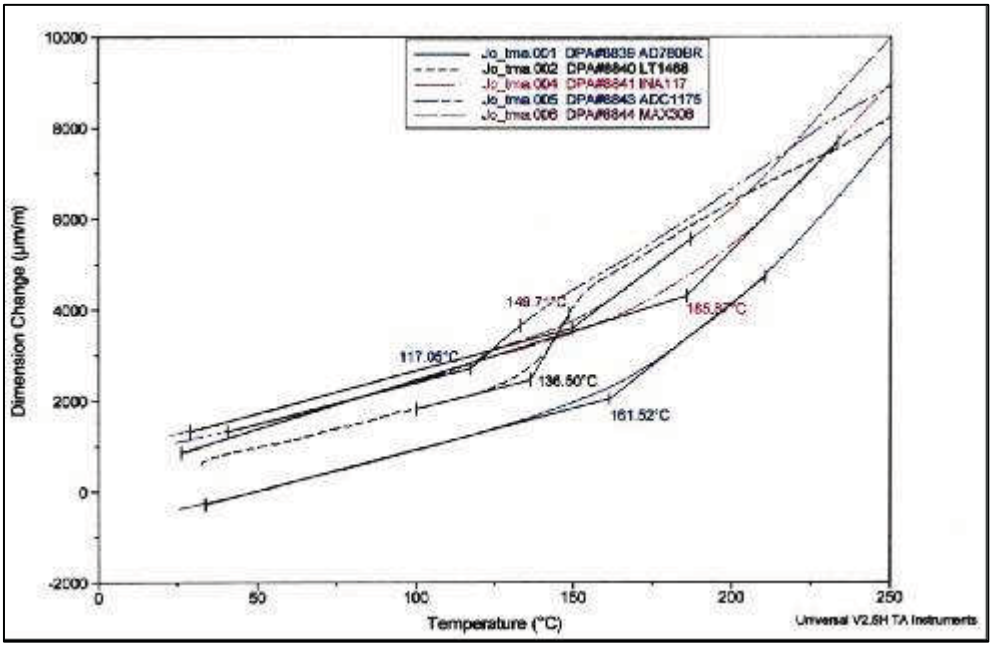

Figure 11. Typical Tg measurements from a variety of PEMs [11].

5.2 Thermal Dissipation for 3D Stack Packages

A major concern in the adoption of 3D architecture is the increased power densities that can result from placing one computation block over another in the multilayered 3D stack. Because power densities are already a major bottleneck in 2D architectures, the move to 3D architectures could accentuate the thermal problem. Even though 3D chips could offer some respite due to reduced interconnect power consumption (as a result of the shortening of many long wires), it is imperative to develop thermally aware physical design tools. For example, partition design may place highly loaded, active gates in a layer close to the heat sink. Thermal issues are more important in ASIC designs than in field programmable gate array (FPGA) architectures because the power densities in ASICs are higher. This is because both the operating clock frequencies and the density of the logic used are much higher in ASICs than in FPGAs [14].

Chip cooling techniques can be divided into two categories. One of these is heat sink optimization, which attempts to cool the heat sink through packaging-level cooling techniques such as fans and micro-channels. However, in 3D designs, the poor thermal-conducting inner layer dielectric (ILD) layers of the stacked chips impede internal heat dissipation from the heat sources to the heat sink.

Optimizing the internal heat dissipation paths is one of the best thermal dissipation techniques for 3D. This includes temperature-aware physical design tools, thermal via insertion, and 3D integrated circuit (IC) micro-channel techniques [15]. Thermal effects are exacerbated in 3D ICs due to higher power density and greater thermal resistance of the insulating dielectric. This can cause degradation in device performance and chip reliability. It is therefore essential to develop 3D-specific design tools that take a thermal co-design approach to address the thermal effects and generate reliable and high-performance designs.

Thermal design is more complex in 3D ICs than in 2D ICs, as the heat flux might increase proportionally to the number of active layers. Without adequate care, this can lead to elevated temperatures, which can lead to reliability failures, such as electromigration, or to timing failures as logic cells might be hotter and slower than assumed. Particular care has to be taken with dock distribution to ensure that the dock buffer temperatures are well known. Because clock buffers are operating all the time, they can easily be hotter than the surrounding logic, and many thermal evaluation tools will not accurately predict the temperature of this relative handful of transistors. Thermal design is particularly difficult in silicon-on-insulator (SOI) design due to the absence of a heat-spreading substrate. Additional TSVs can sometimes be used in the power and ground grids to aid in local heat spreading.

Figure 12 shows an example of a detailed temperature map for one layer of a 3D IC The “tent poles” in this map coincide with locations of the clock buffers. A coarser thermal tool would not resolve these higher temperature points.

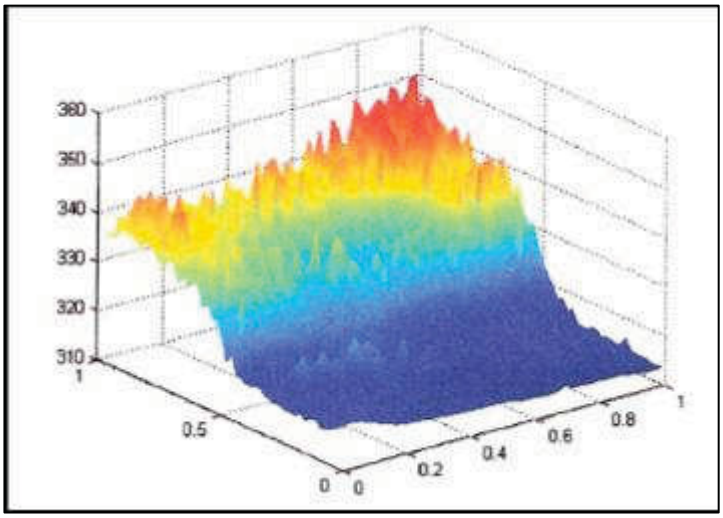

Figure 12. Temperature profile of one chip within a 3D stack [16].

I/O planning is also more complicated in 3D design than in 2D design. Usually, the most power-hungry chip in the stack is placed near the heat sink. Thus, the I/O solder bumps or wire bonds will be placed on a chip further down in the stack that draws less power. The current needed by the most power-hungry chip has to be delivered through the rest of the stack, and high-speed I/O must also be provided. Careful design of the delivery via structures will be needed to ensure high-quality power and signal integrity. For the purpose of maximum 3D integration, standard air-cooled heatsinks will be unable to cope with the power density of these systems. Recent work has focused on implementing micro-fluidic channels [17] onto the backs of 3D-stacked ICs to more effectively remove heat using liquid-phase fluids.

5.3 Destructive and Non-Destructive Characterizations

5.3.1 Optical/SEM Microscopy Characterization

Packages are usually inspected visually using an optical microscope to determine quality and workmanship conditions. Similarly, optical inspections determine solder joint conditions for packages such as quad flat with visible solder joints. Optical micrscopy has limited use for inspection of flip-chip die with fine solder balls and area array attachment. Scanning electron microscopy (SEM) is another tool available for 3D stack packages with fine-pitch and ball attachment evaluation. The x-ray capability of SEM also allows material characterization of surface finish and solder balls to determine if they meet specific requirements such as an absence of pure tin surface finish. Because of size limitation, SEM may not accommodate characterization of assembled packages.

5.3.2 X-Ray Evaluation for PEM/3D Stack

Real-time x-ray systems are categorized as 2D and 3D x-ray systems. The 2D system is a standard x-ray inspection system with a microfocus source and a stationary image intensifier as the detector, capable of producing offset pseudo 3D features. The 2D system has stationary microfocus source intensity, but the detector has off-axis rotational capability. The transmission x-ray captures everything between the x-ray source and image intensifi-

er since x-rays are emitted from the source and travel through the sample. The higher the density of the sample (e.g., solder balls in plastic ball grid arrays (PBGAs), the fewer x-rays will pass through and be captured by the image intensifier. The detected x-rays are displayed in grayscale images, with the lower density (such as voids) areas appearing brighter than the higher density areas. The voltage and current of the x-ray's intensity can be adjusted to reveal features of most sections of the sample.

The 2D x-ray systems are very effective in testing single-sided assemblies. With the use of a sample manipulator, an oblique view angle enhances inspection of both single- and double-sided assemblies with some loss of magnification due to increase in distance between source and detector. Experience is needed in discerning between bottom-side board elements and actual solder and component defects. This can be very difficult or even impossible on extremely dense assemblies. In any case, only certain solder-related defects such as voids, misalignments, and solder shorts are easily identified by transmission systems. However, even an experienced operator can miss other anomalies such as insufficient solder, apparent open connections, and cold solder joints.

The x-ray system with a rotational detector allows oblique generation of x-ray images with a higher magnification and a better intensity resolution since the focal spot remains the same and there is, therefore, no loss of magnification. An isocentric manipulator keeps the field of view unchanged when the oblique view mode is used. This feature allows better characterization of some defect features, including wettability and void location in area array packages.

X-ray techniques have shown to be effective in detecting voids and other internal anomalies of single die packages, especially area array packages. This effectiveness is reduced for 3D packages because of the interference of x-rays from various layers of die within the package and various stack packages.

5.3.3 CSAM Inspection for Voiding/Delamination of PEMs/3D Stack

PEM reliability may be impacted by mold compound adhesion to the various elements within the device, especially the die surface. In this report, the term voiding is used for unintended spaces within the PEM that are present immediately after part manufacture. The term delamination is used when spaces occur or become exacerbated after the part has been manufactured due to storage, board soldering (for example, popcorning), or mission environments.

Die cracks may result from improper mechanical handling during the packaging process and these cracks constitute a reliability risk. Initially, this does not result in changes to electrical parameter but may cause permanent failure during repeated thermal cycling.

Potential problems with plastic packages may be detected using a nondestructive technique: C-mode scanning acoustic microscopy (C-SAM). This method utilizes reflection-mode (pulse echo) technology, in which a single, focused acoustic lens mechanically raster-scans a tiny dot of ultrasound over the sample. As ultrasound is introduced into the sample, a reflection (echo) is generated at each subsequent interface and returned to the sending transducer for processing. Proper lens selection and high-speed digital signal processing allow information to be gathered from multiple levels within a sample. Images can be generated from specific depths, cross sections, or through the entire sample.

If problems are seen in C-SAM testing, a cross-section should be considered to more completely determine the seriousness of the problem. C-SAM provides nondestructive detec-

tion of voids or delamination between lead frame, die face, paddle, heat sink, cracks, and plastic encapsulant. C-SAM may be used effectively for individual packages and dies prior to stacking, but becomes less effective for 3D stack package damage detection.

5.3.4 Cross (X)-Sectional Verification

After use of non-destructive evaluation, x-sectioning may be required to determine hidden features of 3D stack packages or to verify nature and depth of defects observed by C-SAM and x-ray characterizations. X-sectioning easily determines features, such as surface finish thickness and existence of microcracks, which are difficult to detect by other methods. SEM can be used for further analysis of a microsectioned package and assembly. X-sectioning should be performed after environmental testing of 3D packages to better define failure mechanisms even though it is time consuming. This is especially true if source of failure is unknown and cannot be determined by other techniques prior to cross-sectioning.

5.4 Warpage of 3D Package/Assembly

Understanding the package warpage behavior is essential to achieve high package stack yield of PoP. Basically, PoP is a fine-pitch ball grid array (FBGA) stack on the top ball pads of a miniaturized PBGA. The warpage behavior of FBGA and miniaturized PBGA during the reflow process will determine the stacking yield. In traditional package design, the warpage direction (convex or concave) is not of concern as long as the coplanarity can meet the customer's criteria or Joint Electron Device Engineering Council (JEDEC) standards. However, when the warpage directions of top and bottom package are different, the yield of package stacking will be impacted. Some companies are developing a ball-on-ball (BoB) to accommodate the warpage as shown in Figure 13.

Controlling package reflow warpage is essential to get good surface mount technology (SMT) yield in PoP stacking. Since a package consists of multiple materials of different coefficients of thermal expansion (CTEs) and elastic modulus, it may have smile (concave) or sad (convex) warpage as assembled (see Figure 14). The warpage direction and amount often change during reflow. If the warpage is too large over the liquidus temperature of the solder ball, some solder balls may not touch ball pads and normal joints will not form, leading to a quality failure known as cold open joint. Companies are working to minimize or eliminate the package warpage problem.

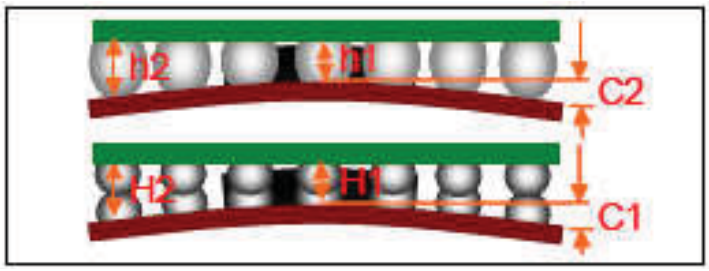

Figure 13. Warpage tolerance of ball-on-pad (BoP) vs. ball-on-ball (BoB).

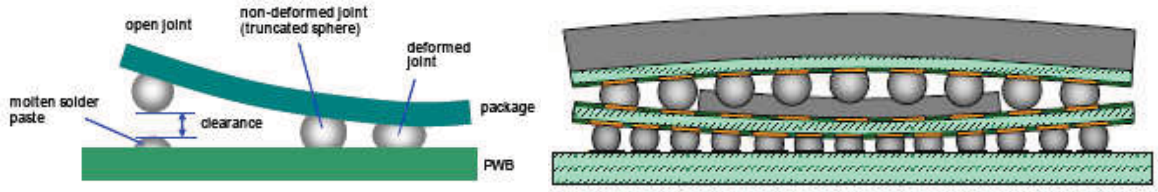

Figure 14. Warpage can affect solder joint reliability at package (*left*) and assembly level (*right*).

5.5 Warpage Measurement Techniques

Warpage, especially behavior with temperature, is an important issue for 3D stack packaging, assembly, and reliability performance. National and international standards organizations are addressing this issue. JEDEC published JESD22B112, High Temperature Package Warpage Measurement Methodology, a specification covering measurement conditions and data presentation using thermal shadow moiré.

Thermal shadow moiré is perhaps the most commonly employed metrology for conducting elevated temperature warpage measurements. Measurements are conducted by placing the Ronchi ruled grating and sample of interest into a thermally insulated enclosure. A heat source is then used to ramp the temperature of the sample under test. A shadow of the reference grating is cast onto the surface of the specimen below by projecting a beam of white light at a specified angle through the grating. Moiré fringe patterns are produced as a result of the geometric interference pattern created between the reference grating and the shadow grating. The Ronchi grating line spacing and overall planarity of the glass substrate are generally invariant to changes in temperature. Thermal shadow moiré measurements are successfully conducted and recorded as the temperature of the sample is increased to the peak reflow temperature and returned to near room temperature.

5.6 Assembly and Reliability Evaluation

Thermal and mechanical acceleration tests are generally performed to determine integrity of electronic systems for general or specific application. There are many reasons to perform an accelerated environmental verification and testing program for electronic assemblies, including:

- Qualification of design for in-service conditions
- Modeling of in-service condition to project life
- Definition of manufacturing variables and their effects
- Screening for manufacturing defects
- Demonstration of quality and reliability of a design
- Demonstration of suitability for the intended use

For electronics in commercial applications, thermal cycling tests are commonly performed to simulate on/off conditions. However, most electronic systems are exposed to other environments, including mechanical fatigue and random vibration. For example, vibration occurs during transportation and mechanical fatigue occurs by repeated use of key punching for portable electronics. Occasional high shock could occur due to acciden-

tal drops. Drop test and mechanical fatigue are now considered for qualification of electronic assemblies especially for newer chip-scale package (CSP), wafer-level package (WLP), and 3D package assemblies and for ranking of lead-free solder alloys.

In addition to much harsher thermal requirements for high-reliability applications, assemblies are generally required to meet severe dynamic loads and vibration fatigue cycling. Therefore, there is a strong need to understand assembly behavior under such stress conditions. The NASA Electronics Parts and Packaging (NEPP) Program team has performed extensive work [18–26] to address both thermal and mechanical behavior of fine-pitch and high-input/output (I/O) ball grid arrays (BGAs) and CSPs. However, assembly and reliability test data for 3D stack packages are scarce and limited to those generated for commercial applications with more benign environmental requirements.

6. NASA Applications

This report covers a literature survey on packaging technology trends for 3D stack packages, qualification and evaluation methodologies for packages, and key quality and reliability issues when they are assembled onto printed wiring boards (PWBs). In general, for space and military grade parts, most qualification and screening processes are intended to detect poor-quality lots and screen out early random failures. For commercial-off-the-shelf (COTS) parts, however, appropriateness of quality is unknown for space applications; therefore, limited improvement in reliability may be achievable depending on the quailty of the COTS flight lot. Also, due to unknown quality and use of a variety of materials, processes, and technologies to design and produce plastic encapsulated materials (PEMs)— most 3D stack packages — any test process developed based on a previous technology may not accelerate and detect all failure mechanisms for a newer device and packaging technology. PEMs should be used only when, due to performance requirements, no alternative high-reliability part exists and projects are willing to accept higher risk.

Upscreening can be implemented to validate acceptability of only the PEM lot being tested, and results may not be extrapolated to other lots. Part manufacturers do not endorse upscreening or use of any commercial part beyond their commercial data sheet specifications. Liability (including adverse publicity) associated with failures of PEMs used in space applications have prompted suppliers to publish disclaimers in their product literature and modify their terms of sale. For these reasons, the user will accept responsibility for failure and associated risk if parts are tested or used in a different manner than what the manufacturer intended.

Using parts outside their design performance parameters and temperatures can reduce built-in reliability margins and/or design robustness. There is also potential risk of introducing latent damage (e.g., ESD) during the handling and testing of devices, which can compromise long-term reliability. Nevertheless, upscreening has been demonstrated to add value. PEM selection should include an extensive review of part manufacturer reliability testing (these tests often include life tests, extended temperature cycling, biased humidity, autoclave tests, high temperature bake, thermal shock, and highly accelerated stress tests [HASTs]).

For all COTS packages, qualification by flight heritage or similarity is not acceptable. Commercial PEM manufacturers produce the same part number with die sourced from different wafer fabs having different die revisions. The package may also be made by multiple production facilities. However, the history of parts' application is important and allows addressing specific problems of design and technology of the parts revealed previously.

Key evaluation characterization of PEM/COSTS 3D stack package includes characterization of glass transition temperature (Tg), visual inspection and serialization of package, radiation analysis, preconditioning and electrical measurements, life testing, extended temperature cycling, destructive physical analysis (DPA), and HASTs. Step-by-step upscreening is summarized below:

- Purchase from authorized part distributor to avoid counterfeits.

- Select PEM parts only from a screened lot.
- Log qualification test results into the PEM database.
- Assess radiation hardness of the parts on a lot-specific according to the mission requirements.
- Evaluate worst-case Moisture Sensitivity Level (MSL) of PEM molding materials to define appropriate bake (or appropriate storage conditions such as dry nitrogen storage or storage in dry bags) prior to soldering to boards. Moisture in PEM can cause damage, including popcorning, during solder reflow.
- Tailor conditions of the temperature cycling, HAST, and high-temperature life testing (HTOL) to ensure that these conditions at least envelop the specifics of the device application. Develop guidelines for application-tailored qualification testing of PEMs.
- Limit the junction temperature to the absolute maximum rated junction temperature for the part. If test temperature causes the maximum rated junction temperature to be exceeded, the test temperature should be decreased appropriately.
- Perform temperature cycling after HTOL testing on the same samples only for economic reasons.
- Perform C-SAM evaluation to estimate damage to the part due to temperature cycling and reflow simulation (or resistance to soldering test) by comparing acoustic images with the baseline measurement results. This test has been found to be unnecessary for standard surface mount packages (SOICs) in standard novolac epoxy compounds.
- Perform failure analysis on any failures during qualification tests to determine whether they are caused by lot-related defects, manufacturing process problems, or improper testing. If no failures are observed, a special evaluation (DPA) should be performed to ensure that no degradation of wire bonding, cratering, and mechanical damage to glassivation and metallization systems occurred.

In addition for 3D stack packages, the effect of temperature rise due to condense power distribution that results from placing one computational block over another, shall be considered during screening and temperature derating. If significant temperature rise due to localize heat dissipation is not adequately designed or screened for, then, this can lead to reliability failures, such as electromigration, or to timing failures as logic cells might be hotter and slower than what was assumed.

Understanding 3D stack warpage behavior both individually and also during stacking of PoP, generally stack of a fine-pitch ball grid on another one, is essential to achieve high package stack yield. In addition to package design and coplanarity requirement, the warpage direction (convex or concave) during reflow might also be of concern and needs to be established prior to assembly. The thermal shadow moiré is commonly used for warpage measurement at elevated temperature.

The 3D packages currently offered for high reliability applications generally provide assembly robustness through use of lead rather than area array solder attachment. However; these packages may be non-hermetic or use polymeric materials that may be sensitive to moisture and degrade with thermal storage and elevated temperature exposures. Exposure to elevated temperature during reflow assembly may causes package failure due

to undesirable rapid temperature excursion during reflow or exceeding glass transition of materials. User shall carefully review for such anomaly even though packages considered as "high reliability application" 3D stack packages.

In addition, since assembly and reliability data are currently lacking for majority of 3D stack packaging technology, the qualification approaches developed under the NASA Electronic Parts and Packaging (NEPP) Program for electronics packaging and assembly shall be followed until specific data for 3D packages are generated. Guidelines developed for high-input/output (I/O) and low-pitch plastic ball grid array (PBGA) packages assembled onto PWBs shall be reviewed since most 3D COTS packages come in area array format. Prior to design of 3D stack packages, it is recommended to review numerous industry standards written for package and assembly of plastic area array packages, including IPC 7095 and IPC 97xx (including 9701A) addressing qualification approaches for thermal and mechanical characterizations.

It is critical to review requirements and best practices established by National Aeronautics and Space Administration (NASA) specifications, including NASA-STD-8739.3 (Soldered Electrical Connections) and NASA-STD-8739.2 (Workmanship Standards for Surface Mount Technology). Pay careful attention to requirements for quality and process controls as well as materials and processes and acceptance for solder and soldering processes. Applicable guideline documents for devices, as well as ball grid arrays (BGAs) and chip-scale packages (CSPs) published under the NEPP Program (http://nepp.nasa.gov), should also be reviewed. For vibration, review force limited vibration testing, NASA-HDBK-7004B, http://standards.nasa.gov.

Recommendations for NASA mission implementation using 3D stack packages are as follows:

- Ensure that all constraints on the use of PEMs are well understood for each specific 3D package.
  - ✓ Use packages offered for high reliability applications including those described in this report, if possible. Be aware of weak points of these packages including being PEM, non-hermetic, using low temperature materials, limitation on stacking, area array packages, and radiation.
  - ✓ No pure tin finish is allowed. Use of lead-free alloys shall be approved for applications.
  - ✓ Use hot air solder leveling (HASL) surface finish for PWB and avoid immersion gold on Ni or other exotic finishes especially for 3D stack with area array packages.
- Define the overall NASA mission environmental requirements, including radiation, mechanical, thermal, life cycle, mechanical shock, vibration, etc.
- Define appropriate potential package technology and types, including 3D stack packages. Review build up, materials, solder geometry and alloys, heat distribution, etc. using package supplier data and application notes.
- Determine if 3D stack package properties are within the envelope of mission environmental requirements in order to avoid early overstress failures. Examples include radiation capability of die, temperature limits of package materials including softening temperature (glass transition temperature, Tg), and junction temperature with con-

sideration of lack of heat dissipation. Determine if special handling, bake out, assembly process, and tools are required.

- For life thermal cycle qualification, determine life cycle requirements for mission. For the purpose of further narrowing 3D package selection, consider the following four categories of NASA missions.
  - ✓ A: Benign thermal cycle exposure with short mission duration (e.g., Space Shuttle Missions)
  - ✓ B: Benign thermal cycles with long mission duration (International Space Station, Hubble Space Telescope, Mars Reconnaissance Orbiter [MRO], Grail, etc.)
  - ✓ C: Extreme thermal cycles with short mission duration (Mars Exploration Rover [MER], etc.)
  - ✓ D: Extreme temperature cycle exposure with long mission duration (Next Generation Space Telescope [NGST], Mars Science Laboratory [MSL], etc.)
- If details on life cycle requirements are not available, then use the following rules-of-thumb to estimate the number of accelerated thermal cycles for NASA missions.
  - ✓ For A and B missions, thermal life cycle requirements are estimated to vary from 100 to 500 accelerated cycles in the range of −55°C to 100°C (NASA cycle).
  - ✓ For C and D missions, estimate the flight allowable temperature ranges and multiply mission cycles by 3. If mission cycle duration is short, add an additional 20 NASA cycles to include the cycle consumption for ground testing.
- Review heritage and package supplier's data for package- and second-level solder joint reliability. Use the following generic guidelines for meeting the requirements.
  - ✓ Limited flight heritage data may be available for 3D stack packages with "high reliability" category.
  - ✓ No flight heritage exists for high-area array 3D stack technology including PBGAs. Generally, the package-on-package stacking category may have adequate thermal cycle resistance, but their resistance to shock and vibration are limited and may be inadequate.
- If available, use a daisy chain package as the test article for accelerated thermal cycle tests as specified in IPC 9701A. Daisy chain packages are generally built using similar materials and layup as the functional package with the exception of using a dummy die with even/odd pad connections.
- Optimize reflow thermal profile, especially for a mixed 3D package technology assembly. Remember that process optimization and process control are key parameters that control solder attachment integrity for 3D stack area array packages, not optical/visual inspection, as commonly used for most other electronic packages at NASA. Refer to NASA standards for use of flux, solder paste quality test, and cleanliness requirements.
- Perform real time x-ray and optical inspection, if possible. Use of an x-ray machine with laminography capability is recommended.

- Prior to x-sectioning, SEM evaluation of the outer rows of package assembly should be performed to reveal damage not detected by optical microscopy. X-section should be performed to reveal internal damage and crack formation.

In summary, following stringent screening procedures developed for implementation of PEM, including additional screening required for assuring stacking quality, determining interactions due to stacking packages, and optimizing assembly processing, it is possible to mitigate most risks associate with implementing 3D stack package technology for NASA applications.

7. Recommendations for Future Evaluation

The literature survey identified only two 3D stack technologies that were previously characterized by the National Aeronautics and Space Administration (NASA), but continuous development in technology requires that they be revisited. In addition, it becomes apparent that significant progress has been made by commercial industry on 3D stack technology and now a number of commercial-off-the-shelf (COTS) 3D packages are matured enough for package and assembly reliability characterization. This report only provides a brief discussion on 3D integration with through-silicon vias (TSVs) since this technology is yet to be fully developed as shown by experts comparing 3D technologies (see Figure 15). In addition, the TSV was the subject of another NEPP body of knowledge (BoK) report [28].

In general, it is recommended to perform tests in order to determine key parameters affecting quality and reliability, to assemble packages onto printed wiring boards (PWBs) in order to narrow process parameters for optimization, and to evaluate assembly reliability under various environmental conditions. Specifically, the most promising 3D packaging technologies for further evaluation are:

- 3D Plus technology: Revisit and identify new changes to determine if additional package characterizations are required. For example, new packages with area array configurations are now offered in addition to conventional system-on-package (SOP). Perform assembly reliability evaluation with emphasis on solder joint integrity. Perform tests with package underfill/corner staking to achieve optimum condition for improvement both under thermal cycle and shock and vibration conditions.

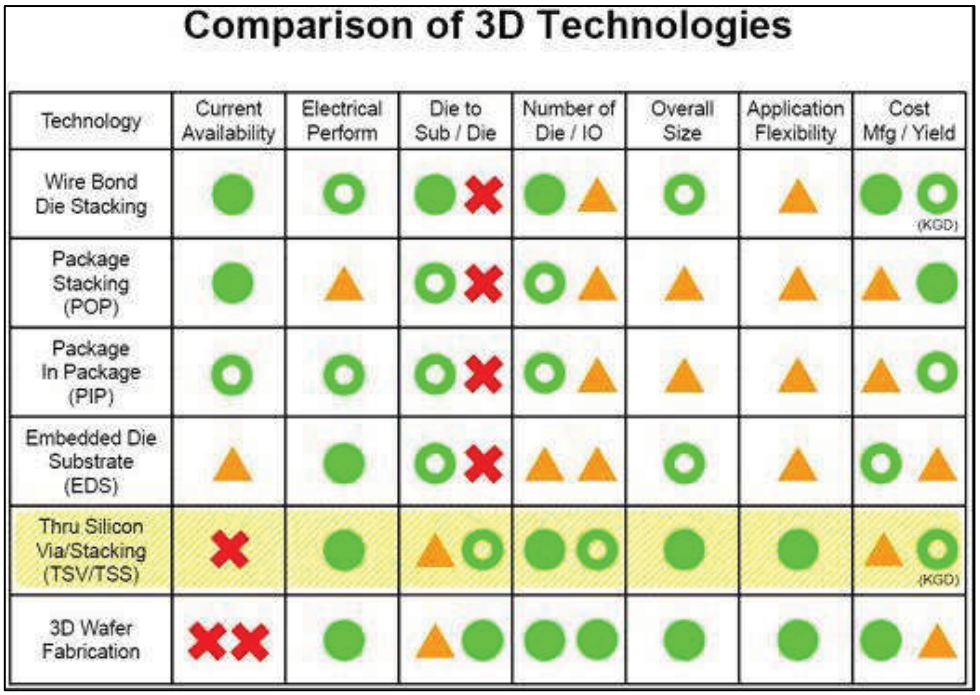

Figure 15. Comparison of 3D technologies presented by Tom Gregorich, Vice President IC Package Engineering, Qualcomm [27].

- Maxwell Technology: Revisit and identify key packaging and assembly issues and provide a process optimization for NASA use. Collaborate with manufacturer to ensure process implementation for achieving high-quality and reliable assemblies.
- Package-on-packages (PoPs) now available for assembly and solder joint reliability characterization: Perform package evaluation as well as assembly process optimization with subsequent reliability evaluation under both thermal and mechanical cycling loading to determine key failure mechanisms and quality assurance indicators.
- Through-mold-via package identified as a package with minimum warpage issue: Reliability test results gathered by manufacturer will be present at SMTA 2009 conference. Results will be reviewed and additional testing will be proposed for reliability evaluation appropriate for high-reliability applications.
- Package in package, especially the wire-bonded stack, are mature and may only need evaluation to understand interaction of board and package and to determine if stacking causes internal wire bond issues under severe mechanical testing.

In summary, this survey clearly identified that NASA has been progressive in evaluating COTS packages with single die and advanced and fine-pitch area array package assembly reliability. Now, because of the industry move to wider usage of 3D packaging, it is recommended to include relevant advanced 3D package and assembly reliability in the NASA Electronic Parts and Packaging (NEPP) Program activities.

8. Acronyms and Abbreviations

AAP	area array packaging
ASE	Advanced Semiconductor Engineering, Inc.
ASIC	application-specific integrated circuit
ASTM	American Society for Testing and Materials
BGA	ball grid array
BoB	ball-on-ball
BoK	body of knowledge
CBGA	ceramic ball grid array
CMOS	complementary metal oxide semiconductor
CNES	Centre National d'Etudes Spatiales
COTS	commercial-off-the-shelf
C-SAM	C-mode scanning acoustic microscopy
CSP	chip-scale (size) package
CTE	coefficient of thermal expansion
CTF	cycles to failure
CVCM	collected volatile condensable materials
Cu	copper
DPA	destructive physical analysis
DSP	digital signal processor
DRAM	dynamic random access memory
ECBU	embedded chip build-up
EDX	energy dispersive x-ray
EEPROM	electrically erasable programmable read only memory
EMC	epoxy mold compound
ESA	European Space Agency
FBGA	fine-pitch ball grid array
FCBGA	flip-chip ball grid array
FPBGA	fine-pitch BGA, a.k.a. chip-scale package (CSP)
FC/DCA	flip-chip direct chip attach
GSFC	Goddard Space Flight Center
HAST	highly accelerated stress test
HDI	high-density interconnect
HTOL	high-temperature life testing
IC	integrated circuit
ILD	inner layer dielectric
I/O	input/output
IPC	Association Connecting Electronics Industries
ISM	internal stacked module

IR	infrared
JPL	Jet Propulsion Laboratory
JEDEC	Joint Electron Device Engineering Council
KGD	known good die
LCP	liquid crystal polymer
LGA	land grid array
MIP	mandatory inspection point
MLF	microlead frame
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
Ni	nickel
PBGA	plastic ball grid array
PEM	plastic encapsulated materials
PiP	package-in-package
PoP	package-on-package
PSvfBGA	package stackable, very thin fine-pitch BGA
PSfcCSP	Package stackable, flip-chip CSP
PTH	plated-through hole
PTHV	PTH via
PWA	printed wiring assembly
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pad
RT	room temperature
SAM	scanning acoustic microscopy
SDRAM	synchronous dynamic random access memory
SEM	scanning electron microscopy
SiP	systems-in-a-package; see PiP
SMD	surface mount device
SMT	surface mount technology
SOC	systems on chip
SOI	silicon on insulator
SOP	system on package
TC	thermal cycle
TCE	thermal coefficient of expansion; also CTE
Tg	glass transition temperature
TMA	thermal mechanical analysis
TML	total mass loss
TMV™	through-mold via
TSV	through-silicon via
TV	test vehicle

WLP	wafer-level package
WLCSP	wafer-level, chip-scale package
WVR	water vapor regained

9. Acknowledgments

The authors would like to acknowledge many people from industry and the Jet Propulsion Laboratory (JPL) who were key to the progress of this activity. The author extends his appreciation to program managers of the National Aeronautics and Space Administration Electronics Parts and Packaging (NEPP) Program, including Michael Sampson, Ken Label, Charles Barnes, and Phillip Zulueta for their continuous support and encouragement.

10. References

1. Smith, L., "3D Electronics and System in Package Integration," IMAPS Global Business Council Conference, March 8–9, 2009.
2. Vardaman, J., "Market Demands, Applications and Requirement for 3D Packaging and 3D ICs," IMAPS Global Business Council Conference, March 8–9, 2009.
3. http://www.amkor.com
4. Houaron, P., Li, Z., Baldwin, D., Stout, G., and Tessier, T., "Processing and Reliability of New 3D-WLCSP Packaging Technology," *The Proceedings of Surface Mount Technology*. SMTAI, 2008.
5. Woychik, C.G., Fillion, R.A., and Aloise, J. "Reliability Assessment of Embedded Chip Build-UP BGA Packages," *The Proceedings of Pan Pacific*. SMTA, 2007.
6. De Castillo, L., Holland, B., Mcpherson, R., Zhang, T., Hou, Z., Dean, R., and Johnson, R.W. "Ultra-thin, flexible electronics," *The IEEE Proceedings of Electronic Components and Technology Conference,* 2008.
7. Plante, J., "Evaluation of 3D Plus Test Structures." December 12, 2001, http://nepp.nasa.gov/DocUploads/64CB4357-A232-4136-A4EAE5AA219AD1A7/FinalReport_Eval_of_3Dplus_CESAR_Cube_121201.pdf
8. Plante, J., and Shaw, H., "Evaluation of 3D Plus Packaging Test Structures For NASA Goddard Space Flight Center," *Proceedings of the European Space Components Conference*, ESCCON 2002, Toulouse, France, September 24–27, 2002.
9. http://www.maxwell.com/microelectronics/index.asp
10. Teverovsky, A., and Sahu, K., "PEM-INST-001: Instructions for Plastic Encapsulated Microcircuit (PEM) Selection, Screening, and Qualification," NASA/TP—2003–212244.
11. Sandor, M., Agarwal, S., and Peters, D., "NEPP/NEPAG COTS PEMS work for NASA," April 8, 2003. http://hdl.handle.net/2014/38815
12. Savage, R., and Parekh, N., "Characterization of Outgassing Properties of Plastic Encapsulated Microcircuits," NASA Parts and Packaging Program, NASA Goddard Space Flight Center, Greenbelt, Maryland, December 1995.
13. Gallo, A. A., "Effect of Mold Compound Components on Moisture-Induced Degradation of Gold-Aluminum Bonds in Epoxy Encapsulated Devices," International Reliability Physics Symposium, 1990, p. 244.
14. Ababei C., et al., "Placement and Routing in 3D ICs," *IEEE Design and Test of Computers,* 2005, p. 520.
15. Cong, J., et al., "An Automated Design Flow for 3D Microarchitecture Evaluation," *Proceedings IEEE Asia and South Pacific Conference on Design Automation,* 2006, p. 384.
16. Franzon, P. D., Davis, W. R., Steer, M. B., Lipa, S., Oh, E. C., Thorolfsson, T., Melamed, S., Luniya, S., Doxsee, T., Berkeley, S., Shani, B., and Obermiller, K. "Design and CAD for 3D Integrated Circuits," *Proceedings of the 45th Annual Conference on Design Automation Table of Contents*, Anaheim, California, p. 668.
17. Sekar, D., King, C., Dang, B., Spencer, T., Thacker, H., Joseph, P., Bakir, M., and Meindl, J. 3D-IC technology with integrated microchannel cooling. *Proc. IEEE Int. Interconnect Technol. Conf.,* 2008.

18. Fjelstad, J., Ghaffarian, R., and Kim, Y.G. *Chip Scale Packaging for Modern Electronics*. Electrochemical Publications, 2002.
19. Ghaffarian, R., "Chip Scale Package Assembly Reliability," Chapter 23 in *Area Array Interconnect Book*, eds. K. Puttlitz, and P. Totta. Kluwer Academic Publishers, 2002.
20. Ghaffarian, R., "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo. McGraw-Hill, 2004.
21. Ghaffarian, R., "Characterization and Failure Analyses of Lead-Free Solder Defects," Chapter 10 in *Lead-Free Solder Interconnect Reliability Book*, ed. D. Shangguan. ASM International, 2005.
22. Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*. ed. E. Suhir. Springer, 2006.
23. Ghaffarian, R., "Reliability of PWB Microvia for High Density Package Assembly," *International Journal of Materials and Structural Integrity* **2**(1–2): 47–63, 2008.
24. Ghaffarian, R., "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies* **31**(2), June 2008.
25. Ghaffarian, R., Bagheri, S., McCormick, H., and Sterian, I. "Reliability of Lead-Free and Tin-Lead Solders for PBGA Assemblies," IMAPs RF Packaging Workshop, San Diego, September 16–18, 2008.
26. Kannabiran, A., Penmatsa, S.V., Ramkumar, S.M., and Ghaffarian, R., "Effect of Forward and Backward Compatibility of Solder Paste and Component Finish on Fine-Pitch Component Assemblies Using ENIG and ImAg PWB Finishes," ASME, InterPACK '07, Vancouver, Canada, July 8–12, 2007.
27. http://www.semiconductor.net/blog/Perspectives_From_the_Leading_Edge/index.php
28. Gerke, D., "Body of Knowledge for Through-Hole-Silicon Via," NASA Electronics Parts and Packaging (NEPP) report.